REMARKS

Applicant's counsel wishes to thank the Examiner for courtesies extended during a telephonic interview on May 15, 2007. During such interview, details of the Walker reference were discussed with respect the rejections made in the 20 Mar 2007 office action.

Claims 1-70, 74-75, 77, and 82-88 are canceled; claims 89-90 are new; and claims 71-73, 76, 78-81, and 89-90 are pending in the application.

Claims 71 stands rejected for Walker et al. (U.S. 6,888,750) (hereinafter "Walker") in view of Yamazaki et al. (6,693,044) (hereinafter "Yamazaki-1") and Yamazaki et al. (6,759,677) (hereinafter "Yamazaki-2"). Amended claim 71 recites a computer system comprising:

> a signal source arranged to provide a data signal; and
>
> an inverter coupled with the signal source, configured to invert the data signal and arranged to output the inverted signal; the inverter including:
>
> a structure comprising silicon and germanium;
>
> a first transistor supported by the structure, the first transistor comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of first source/drain regions; at least a portion of the first active region being within the structure, the first transistor being a PFET and the first source/drain regions accordingly being p-type doped regions; the

first gate being substantially non-overlapping with respect to the first source/drain regions;

an insulative material over at least a portion of the first transistor;

a first layer of semiconductive material over the insulative material;

a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material;

a second transistor over the insulative material, and supported by the first and second layers of semiconductive material, the second transistor comprising a second gate and a pair of second source/drain regions, the second transistor being an NFET and the second source/drain regions accordingly being n-type doped regions; the second source/drain regions extending into the second layer of semiconductive material; the second gate being directly over the first gate; the second gate being substantially non-overlapping with respect to the second source/drain regions;

the first and second gates being electrically connected to one another, and being in electrical connection with the signal source; and

one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with the output.

The first gate being substantially non-overlapping with respect to the first source/drain regions and the second gate being substantially non-overlapping with respect to the second source/drain regions is supported by, for example, Fig. 11 of the originally filed application, and therefore does not comprise "new matter."

The Examiner cites Figs. 12-14 and accompanying text of Walker as disclosing the signal source, inverter, and output recited by claim 71. The Examiner also cites Fig. 10A and accompanying text of Walker as disclosing a semiconductor structure of a first transistor and a second transistor of the inverter of Fig. 13 as recited by claim 71.

However, the semiconductor structure illustrated by Walker Fig. 10A and accompanying text is not related to the inverter of Walker Fig. 13. In other words, Fig. 13 is not a schematic diagram of the semiconductor structure illustrated in Fig. 10A. Walker provides, in Fig. 1 and accompanying text, a schematic overview of a nonvolatile memory array having three layers. The bottom layer is an SOI substrate 3. The middle layer is a driver circuit 2 formed over insulative surface 3. Finally, a top layer comprising nonvolatile memory devices is formed over the driver circuit layer 2. The driver circuit layer contains read/write circuitry used to write data to the top layer memory devices and to read data from the top layer memory devices. The

top layer contains a regular array of nonvolatile memory devices used to store data supplied by the middle layer (the driver circuit layer).

Fig. 10A is a cross-sectional view of one embodiment of the top layer (the nonvolatile memory device layer). This embodiment comprises charge storage devices having floating gates.

In contrast, Figs. 12-14 illustrate schematic diagrams of one embodiment of the middle layer of Fig. 1 (the driver circuit layer). Consequently, Fig. 10A does not illustrate the circuits schematically illustrated in Figs. 12-14.

Applicant notes that Col. 17 lines 27-44 of Walker disclose that any charge storage device that functions as an antifuse when a conductive link has been formed through its charge storage region may be used within the middle layer (the driver circuit layer). The devices illustrated in Fig. 10A have floating gates used to store charge. These floating gates, however, are not antifuse devices because a conductive link is not formed through the floating gate to the control gate. Thus, the devices illustrated in Fig. 10A are not the type of devices envisioned by Walker for use within the driver circuit layer.

Even if the devices illustrated in Fig. 10A could be used in the driver circuit layer, the devices illustrated in Fig. 10A do not disclose a first gate being substantially non-overlapping with respect to first source/drain regions, or a second gate being substantially non-overlapping with respect to second source/drain regions as recited by amended claim 71.

Applicant notes that Fig. 11 of Walker illustrates a cross sectional view of driver circuit layer related to the schematic diagrams of Figs. 12-14. However, Fig. 11 does not disclose each of the recited elements of claim 71. For example, , Fig. 11 fails to disclose a second layer of semiconductive material physically contacting a first layer of conductive material, a first gate being substantially non-overlapping with respect to first source/drain regions, or a second gate being substantially non-overlapping with respect to second source/drain regions as recited by amended claim 71.

Accordingly, the rejection of claim 71 should be withdrawn.

Claims 72-73, 76, 78-81, and 89-90 depend from claim 71, and are therefore allowable for at least the reasons discussed above regarding claim 71.

New claims 89 and 90 are supported by, for example, Fig. 11 and paragraphs 62-65 and 84 of the specification.

Claims 71-73, 76, 78-81, and 89-90 are allowable for at least the reasons discussed above. Applicant therefore respectfully requests that the Examiner's next action be a Notice of Allowance formally allowing all of the pending claims.

Respectfully submitted,

Dated: 14 Jun 2007

By: Paul Holdaway
Paul S. Holdaway
Reg. No. 56,376